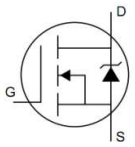
• General Description

It combines planar MOSFET technology with a low resistance package to provide low $R_{DS(ON)}$.

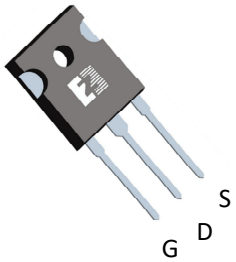
• Product Summary



V_{DS}= 60V
$R_{DS(ON)}$ = 4.2mΩ
I_D= 160A

• Features

■AEC-Q101 Qualified
■Low $R_{DS(ON)}$ to minimize conductive loss
■Low Gate Charge for fast switching
■Low Thermal resistance



TO-247

•Application

■BLDC Motor driver
■DC-DC
■Load Switch

•Ordering Information:

Part NO.	ZMPA070N06HC
Marking	ZMP070N06H
Packing Information	TUBE
Basic ordering unit (pcs)	400

•Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage①	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	160	A
	I_D	T_C=75℃	115	A
	I_D	T_C=100℃	94	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	640	A
Total Power Dissipation	P_D	T_C=25℃	333	W
Total Power Dissipation	P_D	T_A=25℃	3.8	W
Operating Junction Temperature	T_J		-55 to +175	℃
Storage Temperature	T_{STG}		-55 to +175	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	2000	mJ
		L=0.5mH, V_{GS}=10V, Rg=25Ω,	3600	mJ
ESD Level (HBM)	CLASS 2			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.45	°C/W
Thermal resistance, junction-ambient	R_{thJA} ②		-	40	°C/W
Soldering temperature（total time<10s)	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	2.0	2.6	4.0	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 60V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 20A		4.2	6	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V, I_{SD} = 10A		42		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 20A			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	5120	-	pF
Output capacitance	Coss		-	1320	-	
Reverse transfer capacitance	Crss		-	450	-	
Gate Risistance	Rg	f = 1MHz	-	1.2		Ω
Total gate charge	Qg	V_{DD} = 15V, I_D = 20A, V_{GS} = 10V	-	118	-	nC
Gate - Source charge	Qgs		-	12	-	
Gate - Drain charge	Qgd		-	42	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	22	-	ns
Turn-ON Rise time	t_r		-	76	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	98	-	ns
Turn-Off Fall time	t_f		-	30	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=20V, dI_S/dt = 100A/us, I_S=50A	-	105	-	ns
Reverse Recovery Charge	Q_{RR}		-	210	-	nC

Fig.1 Gate-Charge Characteristics

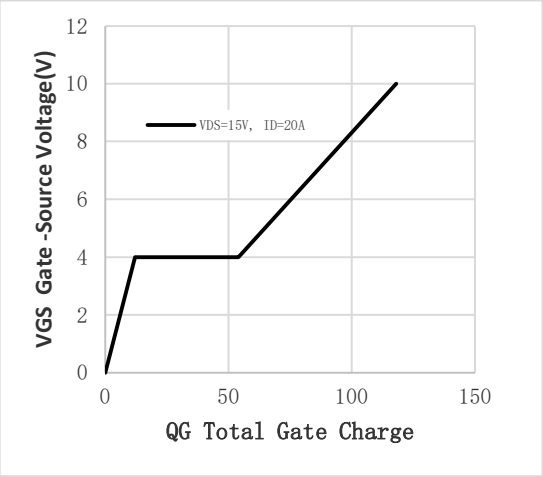


Fig.2 Capacitance Characteristics

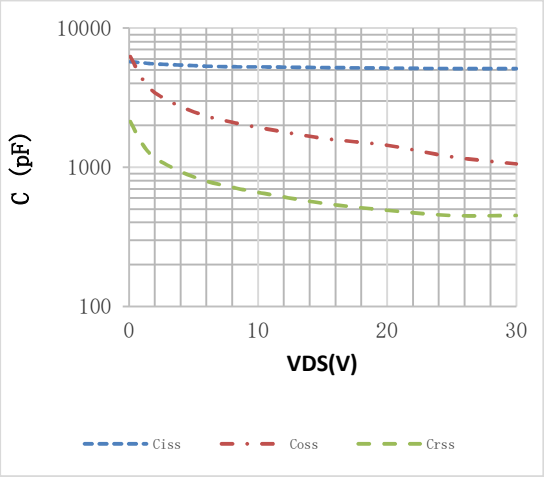


Fig.3 Power Dissipation

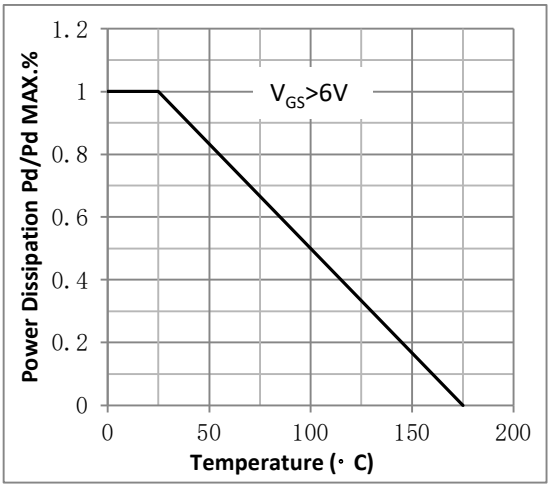


Fig.4 Typical output Characteristics

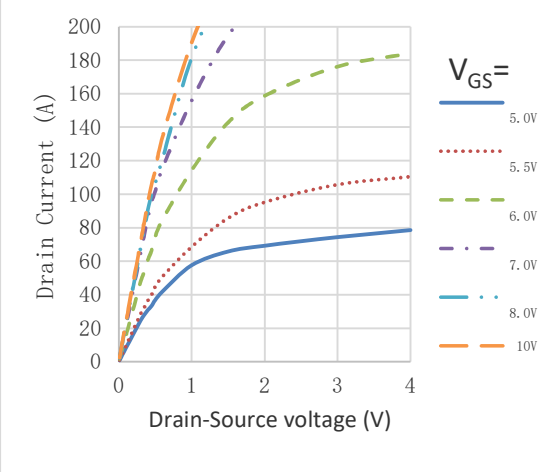


Fig.5 Threshold Voltage V.S Junction Temperature

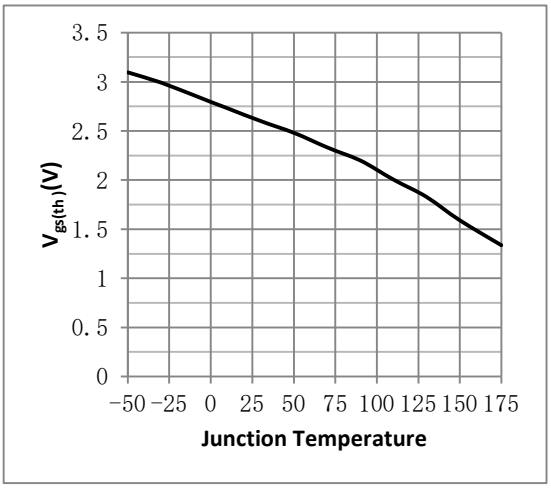


Fig.6 Resistance V.S Drain Current

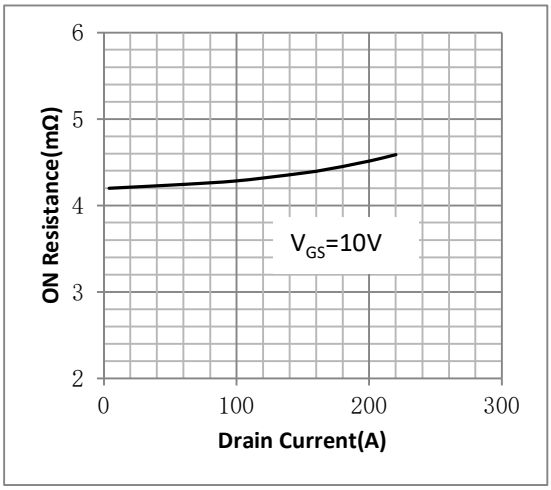


Fig.7 On-Resistance VS Gate Source Voltage

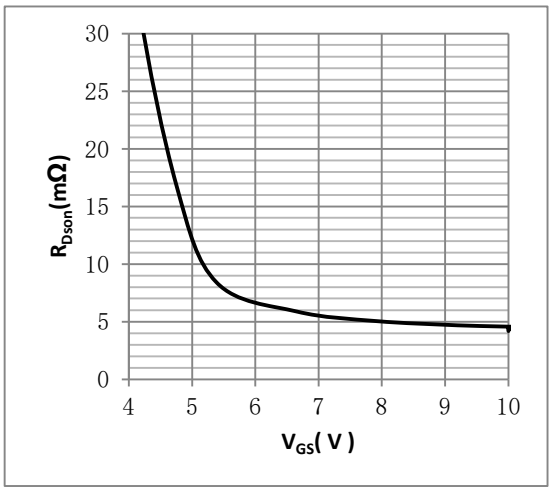


Fig.8 On-Resistance V.S Junction Temperature

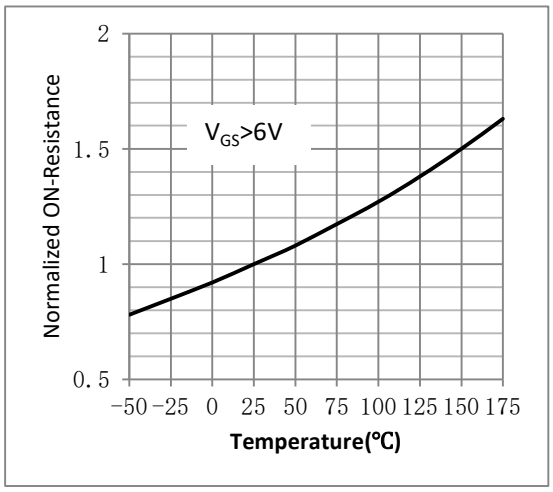


Figure 9. Diode Forward Voltage vs. Current

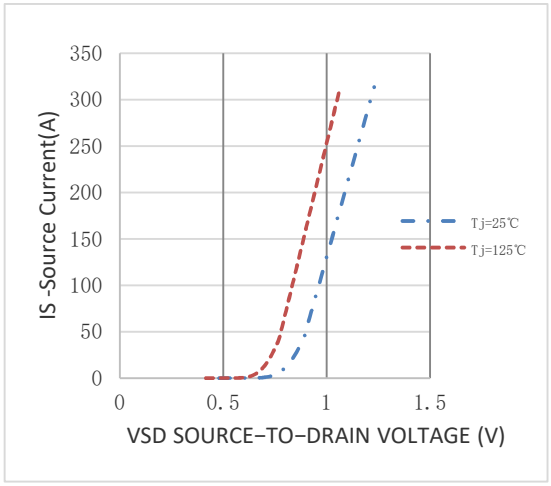


Figure 10. Transfer Characteristics

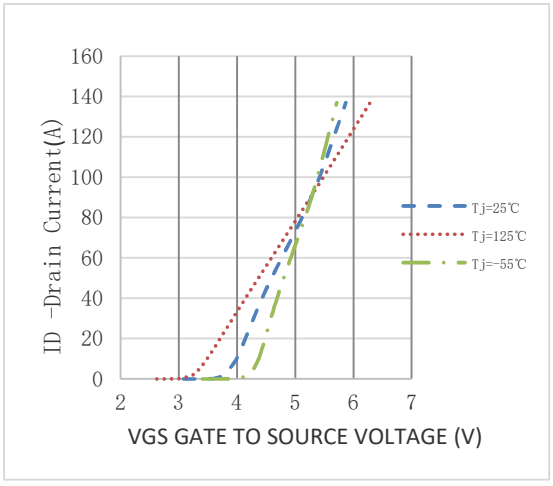


Fig.11 Safe Operating Area

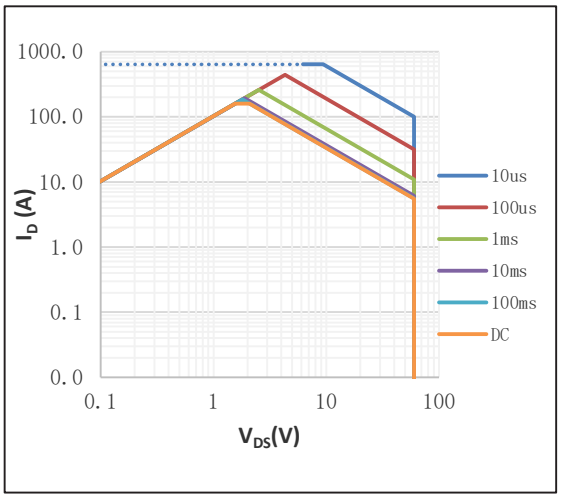
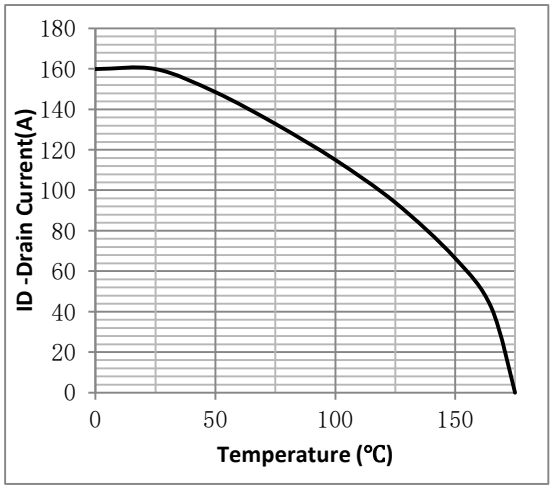
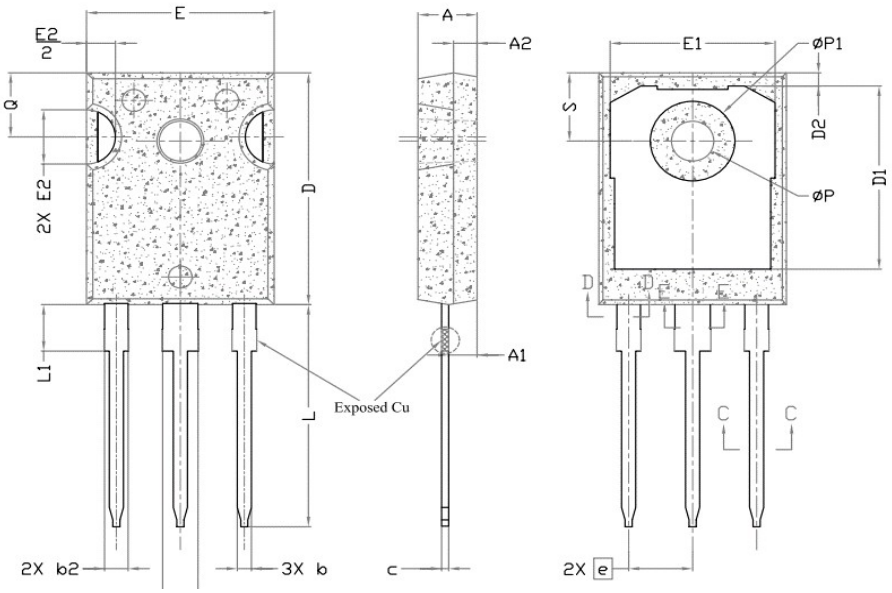


Fig.12 ID vs. Junction Temperature③



●TO-247 Package Outline



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
øP	3.56	3.61	3.65	7
øP1	7.19REF.			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. V_{GS}=10V.

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Revision History

Version	Date	Change
A	2023.10.6	New
B	2024.7.23	Modified vth typical
C	2024.12.13	Update SOA